IN THE CLAIMS:

The following is a complete listing of the claims in this application, reflects all changes currently being made to the claims, and replaces all earlier versions and all earlier listings of the claims:

1. (Currently Amended) A solid-state imaging device of an amplification type, comprising:

a plurality of picture elements arranged two-dimensionally ~~each including a photoelectric conversion element and a transistor for amplification~~, each picture element comprising:

~~wherein~~ a semiconductor light-receiving region of a first conductivity type serving as ~~each~~ a photoelectric conversion element, the light-receiving region being [[is]] disposed in a common well comprising a semiconductor of a second conductivity type ~~formed in a semiconductor substrate of the first conductivity type;~~ , and

~~wherein~~ a semiconductor region of the first conductivity type serving as a source and drain of ~~each~~ a transistor for amplification, the semiconductor region being disposed in the common well; and

~~wherein~~ a plurality of contacts for supplying a reference voltage to the common well, the plurality of contacts being [[are]] disposed ~~inside a picture element array area of the common well~~ between the picture elements or within the picture elements.

2. (Currently Amended) The solid- state imaging device according to claim 1, wherein ~~the plurality of~~ the contacts are disposed ~~inside the picture element array area at determined~~ at predetermined intervals.

3. (Cancelled)

4. (Currently Amended) The solid-state imaging device according to claim [[2]] 1, ~~wherein~~ further comprising a plurality of wirings ~~connected to the contacts~~ for supplying the reference voltage, each wiring being connected to a corresponding one of the contacts and being [[are]] disposed in a row direction or a column direction ~~of the picture element array area~~ between the picture elements or within the picture elements at predetermined intervals.

5. (Currently Amended) The solid-state imaging device according to claim 4 [[2]], wherein the contacts are disposed at ~~for~~ every n rows ($n \geq 1$) of the picture elements ~~element array area~~ and the wirings ~~connected to the contacts~~ are disposed at ~~for~~ every m columns ($m \geq 2$) of the picture elements ~~element array area~~.

6. (Currently Amended) The solid- state imaging device according to claim 4 [[2]], wherein the wirings connected to the contacts are disposed at ~~for~~ every m rows ($m \geq 2$) of the picture elements ~~element array area~~ and the contacts are disposed at ~~for~~ every n columns ($n \geq 1$) of the picture elements ~~element array area~~.

7-9. (Cancelled)

10. (Currently Amended) The solid-state imaging device according to claim 1, wherein the contacts are also disposed outside the outermost picture elements ~~around the picture element array area~~ of the common well.

11. (Currently Amended) A solid-state imaging device of the amplification type, comprising:

a plurality of picture elements arranged two-dimensionally ~~each including a photoelectric conversion element and transistor for amplification~~, each picture element comprising:

~~wherein~~ a semiconductor light-receiving region of a first conductivity type serving as ~~each~~ a photoelectric conversion element, the photoelectric conversion element being [[is]] disposed in a common well of a second conductivity type formed in a semiconductor substrate of the first conductivity type, and

~~wherein contacts for supplying a reference voltage to the common well are disposed around a picture element array area of the common well and in each picture element;~~

~~wherein~~ a semiconductor region of the first conductivity type serving as a source or drain of ~~each~~ a transistor for amplification, the semiconductor region being [[is]] disposed in the common well; [[, and]]

contacts for supplying a reference voltage to the common well, the reference voltage contacts being disposed outside the outermost picture elements and in each picture element;

a wiring connected to the reference voltage contacts for supplying a reference voltage; and

~~wherein~~ a power source contact for ~~a power source for~~ supplying, to the semiconductor region of the first conductivity type, a power source voltage for driving the transistor for amplification, the power source contact being [[is]] disposed [[for]] in each picture element, [[.]]

wherein the power source contact is connected by a wiring to a power source, the power source wiring being separate from the reference voltage wiring.

12. (Currently Amended) The solid-state imaging device according to claim 11, wherein one of either the reference voltage contacts or ~~contact and~~ the power source contacts ~~contact for the power source~~ is connected to a wiring arranged at every row or every column of the picture elements ~~predetermined intervals in the picture element array area~~ and the other of the reference voltage contacts or ~~contact and~~ the power source contacts ~~contact for the power source~~ is connected to a shielding layer having a light-receiving window formed above the wiring arranged at every row or every column of the picture elements.

13. (Currently Amended) The solid-state imaging device according to claim 12, wherein the wiring arranged at every row or every column of the picture elements is connected to the reference voltage contacts and is disposed between two control lines for controlling a semiconductor element inside the picture element.

14. (Currently Amended) The solid-state imaging device according to claim 11, wherein the power source contacts are connected to ~~wirings for the reference voltage arranged inside the picture element array area at predetermined intervals and the contact for the power source is connected to~~ a shielding layer having a light-receiving window formed above the wiring for the reference voltage.

15. (Currently Amended) The solid-state imaging device according to claim 14, wherein the reference voltage wiring ~~for the reference voltage~~ is disposed between two control lines for controlling a semiconductor element in the picture element.

16. (Currently Amended) The solid-state imaging device according to claim 13, wherein ~~at least one~~ each of the picture elements further includes a transfer gate, a transistor for reset and a transistor for selection, and

wherein the two control lines are two selected from the group consisting of a control line of the transfer gate, a control line of the reset transistor ~~for reset~~ and a control line of the selection transistor ~~for selection~~.

17. (Currently Amended) The solid-state imaging device according to claim 11, wherein ~~at least one~~ each of the picture elements further includes a reset transistor ~~for reset~~,

wherein a reset contact ~~for reset~~ for supplying a reference voltage for reset to the reset transistor ~~for reset~~ is disposed ~~for~~ in each picture element ~~provided with the transistor for reset~~,

wherein any two of the power supply contact, the reset contact ~~for reset~~ and the power source contact ~~for the power source~~ are connected to intersecting wirings arranged in the picture element array area, and

wherein the remaining one of the power supply contact, the reset contact ~~for reset~~ and the power source contact ~~for the power source~~ is connected to a shielding film having a light-receiving window formed above the wiring intersecting wiring.

18. (Currently Amended) The solid-state imaging device according to claim 11, wherein the power source contact ~~for the power source~~ is connected to a source or a drain of the selection transistor ~~for selection~~ and supplies the power source voltage to the semiconductor region ~~area~~ through the selection transistor ~~for selection~~.

19-22. (Cancelled)